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SE 10	Sobstitu	te for form 1449/PTO			Complete if Known		
	4				Application Number	10/604,984	
AR STO	INT			SCLOSURE	Filing Date	28 August 2003	-
\$	SYA	TEMENT E	BYA	PPLICANT	First Named Inventor	Razak Hossain	
PATEMI BY	HIS	(Use as many she	ate ae :	*************	Art Unit	2825	
		(USB as many sile	- LD 63 ;	ocessery)	Examiner Name	Naum Levin	
	Sheet	1	of	1	Attorney Docket Number	03-LJ-011	

		NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*	xaminer Cite Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title			
NL		DE, VIVEK et al., Techniques for Leakage Power Reduction, Design of High-Performance Microprocessor Circuits, IEEE Press, Chap. 3, pp. 46-62, 2001		
NL		ALOUL, PADI A., et al., "Robust SAT-Based Search Algorithm for Leakage Power Reduction", International Workshop on Power and Timing Modeling, Optimization and Simulation, Seville, Spain, 2002		
	<u> </u>			

Examiner	None Torris (None York)	Date	40.400.400.40
Signature	Naum Levin /Naum Levin/	Considered	10/13/2006

[&]quot;EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

DOCKET NO. 03-LJ-011 (STMI01-03011) U.S. SERIAL NO. 10/604,964 **PATENT**

SANKARALINGAM, R., et al., "Reducing Test Power During Test Using Programmable Scan Chain Disable," XP010587990, Proceedings of the First IEEE International Workshop on Electronic Design, Test and Applications, January 29, 2002, pages 159-163.

WANG, S., "Generation of Low Power Dissipation and High Fault Coverage Patterns for Scan-Based BIST," XP010609814, ITC International Test Conference, Paper 29.3, Oct. 7-10, 2002, pages 834-843.

SINANOGLU, O., et al, "Test Power Reduction Through Minimization of Scan Chain Transitions," XP-002306228, Proceedings of the 20th IEEE VLSI Test Symposium, April 28, 2002, pages 166-171.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

In accordance with 37 C.F.R. 1.97(e), the undersigned certifies that each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Information Disclosure Statement.

Further, pursuant to 37 C.F.R. § 1.97(e) and the above statements, no fee is believed to be due for the filing of this Information Disclosure Statement.

Respectfully submitted,

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Applicant must present form PTO/SB/08 for the future consideration.

Naum Levin / Naum Levin /

10/24/2006